AMENDMENTS TO THE CLAIMS

1. (Currently amended) A pixel sensor cell comprising:

a pinned photodiode;

a transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode NMOS transistor~~FET~~;

a reset transistor coupled between a high voltage rail V_{dd} and the output node; ~~and~~

an output transistor, the gate of the output transistor being coupled to the output node; and

said pixel sensor cell formed on an integrated circuit having a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor such that charge from said pinned photodiode cannot flow to said output node.

2. (Original) The pixel sensor cell of Claim 1 further including a row select transistor, the gate of the row select transistor being coupled to a row select line, the input of the row select transistor being coupled to the output of the output transistor, and the output of the row select transistor providing the output of the pixel sensor cell.

3. (Original) The pixel sensor cell of Claim 1, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

4. (Cancelled)

5. (Currently amended) The pixel sensor cell of Claim 1, wherein said negative voltage generator generates a $-V_{dd}$ voltage that is applied to said ~~depletion mode~~ transfer transistor to completely turn off said transfer transistor~~has a threshold voltage near V_{dd}~~.

6. (Cancelled)

7. (Currently amended) The pixel sensor cell of Claim 1, wherein the pinned photodiode is a P+/Nwell/Psub structure ~~and said transfer transistor is an N-type MOSFET~~.

8. (Currently amended) The pixel sensor cell of Claim 1, wherein the pinned photodiode is a N+/Pwell/Nsub structure ~~and said transfer transistor is a P-type MOSFET.~~

9.-20. (Cancelled)

21. (New) A method of operating an active pixel, the pixel cell including a pinned photodiode, a transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode NMOS transistor, a reset transistor coupled between a high voltage rail V_{dd} and the output node, and an output transistor, the gate of the output transistor being coupled to the output node, the method comprising:

during an integration period, holding said transfer transistor to a negative voltage such that said transfer transistor is completely off; and

during a transfer period, using a positive voltage to turn on said transfer transistor to allow charge from said photodiode to flow to said output node.

22. (New) The method of Claim 21 wherein said negative voltage is $-V_{dd}$ and which is generated by an on chip charge pump.

23. (New) The method of Claim 22 wherein said positive voltage is V_{dd} such that the swing from the transfer transistor being on and off is between $-V_{dd}$ to V_{dd}.